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APPARATUS FOR SYNCHRONIZATION OF DOUBLE DATA RATE SIGNALING

Abstract Of The Disclosure

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A signal phase shifting circuit shifts the phase of an input signal, such as a STROBE signal, based on a reference signal, such as a CLOCK signal, to facilitate, for example, receiving of double data rate data. The signal phase shifting circuit includes a reference signal period dividing circuit having a feedback delay matching array operatively coupled to one of a plurality of voltage control delay lines. This signal phase shifting circuit also includes a variable delay circuit that provides a phase shifted output signal, such as a phase shifted STROBE signal, that includes a delay stage in a phase shifted output signal drive buffer coupled to the delay stage, such as a voltage control delay line. The feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the phase shifted output signal drive buffer in the variable delay circuit. Accordingly, a more stable STROBE signal phase shift occurs that is less sensitive to temperature and voltage variations while still allowing the compensation of delay due to, for example, printed circuit board layout delays and other delays.